Nanoscale electronics based on two-dimensional dopant patterns in silicon

T.-C. Shen[a)]
Department of Physics, Utah State University, Logan, Utah 84322

J. S. Kline
Department of Physics, Utah State University, Logan, Utah 84322
and Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

T. Schenkel
Lawrence Berkeley National Laboratory, Berkeley, California 94720

S. J. Robinson
Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

J.-Y. Ji
Department of Physics, Utah State University, Logan, Utah 84322

C. Yang and R.-R. Du
Department of Physics, University of Utah, Salt Lake City, Utah 84112

J. R. Tucker
Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

(Received 2 June 2004; accepted 13 September 2004; published 10 December 2004)

A nanoscale fabrication process compatible with present Si technology is reported. Preimplanted contact arrays provide external leads for scanning tunneling microscope (STM)-defined dopant patterns. The STM's low energy electron beam removes hydrogen from H terminated Si(100) surfaces for selective adsorption of PH_3 precursor molecules, followed by room temperature Si overgrowth and 500 °C rapid thermal anneal to create activated P-donor patterns in contact with As^+-implanted lines. Electrical and magnetoresistance measurements are reported here on 50 and 95 nm-wide P-donor lines, along with Ga-acceptor wires created by focused ion beams, as a means for extending Si device fabrication toward atomic dimensions. © *2004 American Vacuum Society.*
[DOI: 10.1116/1.1813466]

I. INTRODUCTION

Lithography, interfaces, and external contacts are three major challenges in developing nanoscale electronics. A few years ago, we proposed selective adsorption of PH_3 molecules onto scanning tunneling microscope (STM) patterned H-terminated Si(100) surfaces to create P-donor electronics embedded into the Si crystal.[1] A major advantage of this approach is the relatively large Bohr radius of dopant atoms, offering the possibility for control of electron tunneling at ~ 10 nm dimensions and greatly reduced lithographic demands for tunnel junctions. We and other researchers have subsequently demonstrated that ultradense P δ-layers can be grown into Si with a fully activated carrier density of $\sim 1 \times 10^{14}$ cm^{-2}, showing metallic conductivity of a two-dimensional electron gas (2DEG) at cryogenic temperatures.[2,3] Schofield *et al.* also demonstrated that STM electron stimulated desorption (ESD) can be used to attach individual PH_x precursors to atomically positioned Si dangling bonds on the otherwise H-terminated surface.[4] In order to realize atom-scale devices as prototypes for a future technology, it will be necessary to integrate this process with standard Si microprocessing. Toward that goal, we have developed a low-temperature UHV process to produce atomically flat and clean surfaces by low energy Ar^+ ion sputtering followed by a 700 °C anneal.[5] In this article, we demonstrate that the complete P-donor patterning process is compatible with preimplanted contact arrays. Nanometer lines defined by STM lithography, and focused ion beam wires, are characterized by electrical and magnetotransport measurements.

II. DEVICE TEMPLATES: PROCESSING AND CHARACTERIZATION

Figure 1(a) shows the schematic for a two-terminal device template consisting of 200 pairs of interdigitated finger contacts implanted with 40–50 keV As^+ ions at a dose of 1×10^{15} cm^{-2}, into a p-type substrate with B doping of 3×10^{17} cm^{-3}. The width of the implanted fingers is 1.25 μm and the gap between them is 0.75 μm. These highly degenerate n^+ lines will serve to connect a P-donor device structure to be fabricated across one of these gaps to external leads, through the top and bottom pads of the implanted array. The activation anneal of 550 °C/5 min is performed in the low vacuum load-lock of our ultrahigh vacuum (UHV) system.

a)Author to whom correspondence should be addressed; electronic mail: tcshen@cc.usu.edu

 ©2004 American Vacuum Society

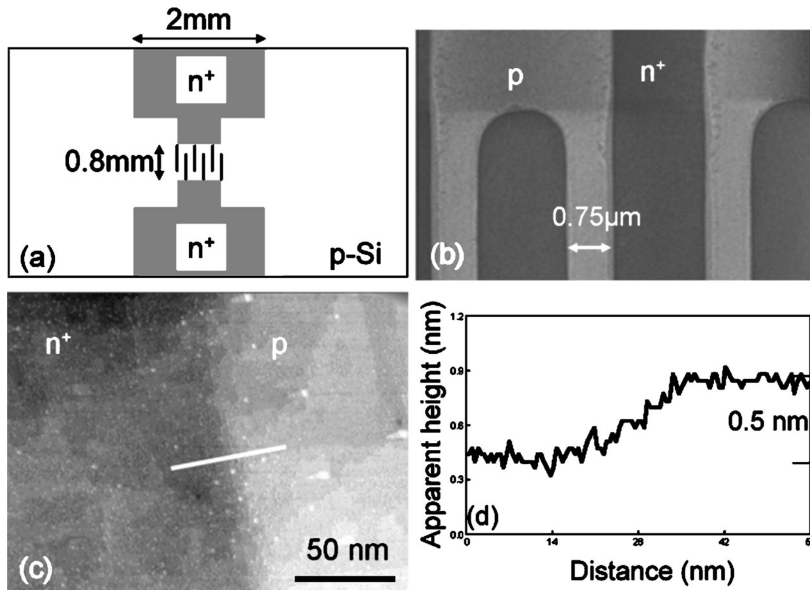

FIG. 1. (a) The schematic of the two-terminal device template. (b) AFM image of a device template. The dark region is As^+ implanted and is 4.3 nm lower than the *p*-type substrate. (c) STM image of a template after UHV processing. (d) A linescan across the boundary between an As^+-implanted finger and the substrate.

Defective templates are screened out at this point by measuring the (nominally open) resistance across the interdigitated finger array at 4.2 K. Measured resistance of a useable template is typically >1 GΩ for a bias range of several volts before breakdown occurs. These templates are subsequently cleaned by the standard RCA procedure[6] and dipped in aqueous HF solution (49%) before being reintroduced into the UHV system. In atomic force microscope (AFM) images, the As^+-implanted fingers are usually lower than the substrate after HF etching, as shown in Fig. 1(b), presumably due to enhanced oxidation and subsequent removal. The amount of surface height difference depends upon the conditions of annealing, wet chemical etching, and the miscut in each particular wafer.

Once inside the UHV, the template's surface is sputtered by 300 eV Ar^+ ions for 1 h in a chamber back filled with Ar to 5×10^{-5} Torr. A residual gas analyzer is used to insure that the impurity level of other reactive gases is $<10^{-4}$. The sputtering rate is $\sim$13 nm/h based on AFM measurements. After Ar^+ ion sputtering, the template is annealed to 700 °C for a few seconds. Finally, a single atomic layer of "H-atom resist" is applied by positioning the sample 6 cm from a hot W-filament in the presence of 1×10^{-6} Torr H_2 for 5 min at $\sim$350 °C. The surface of a typical UHV-processed template is depicted in the STM image in Fig. 1(c), where the darker (lower) region is an As^+-implanted finger. Atomic terraces are clearly visible in both regions. Figure 1(d) shows a line scan across the boundary, indicating a 0.5 nm recess of the As^+-implanted region from the *p*-type substrate that is acceptable for STM lithography. This low-temperature surface preparation technique provides a flat, unaltered surface at *p* -*n* junctions; interesting details will be reported elsewhere.[7]

STM e-beam lithography[8] is used to remove H atoms from the desired pattern, creating bare Si dangling bonds for selective adsorption of PH_3 precursor molecules at room temperature to a saturation density of $\sim$1/4 ML. The P atoms are converted into activated donors by growing $\sim$20 or more atomic layers of Si at room temperature, followed by a rapid thermal anneal to 500 °C. The surface of the overlayer is conformal to the original surface, and STM images indicate good epitaxy. The same process on *un*patterned templates leads to an earlier breakdown of nominally open finger arrays, but the voltage range of >1 GΩ resistance at 4.2 K is still greater than ±2 V, sufficient for nanoscale device fabrication.

III. P-DONOR LINES

To demonstrate that device structures can be fabricated *inside* the Si crystal and connected to macroscopic leads, we

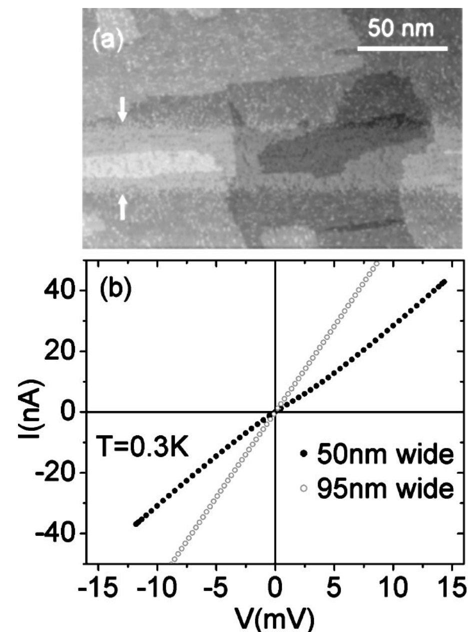

FIG. 2. (a) STM image of a 33 nm wide pattern (between marks) on an UHV processed H-terminated template. (b) *I-V* characteristic of 50 and 95 nm wide, 0.75 μm long P-donor lines at 0.3 K.

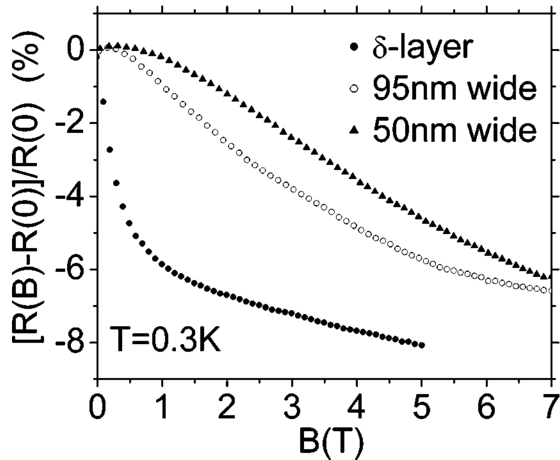

FIG. 3. Magnetoresistance change for a δ-layer, 95 and 50 nm wide P-donor lines at 0.3 K.

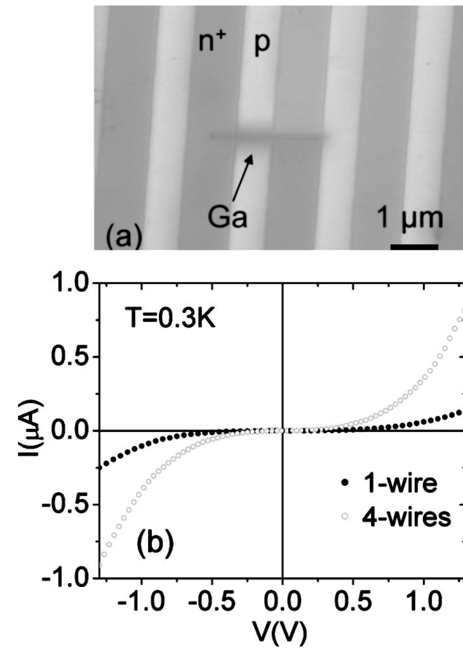

FIG. 4. (a) Electron micrograph of a 200 nm wide Ga-acceptor wire implanted by focused ion beam between two As^+-implanted fingers. (b) *I-V* characteristics of 1 and 4 Ga-acceptor wires, each 200 nm wide, between a pair of As^+-implanted fingers at 0.3 K.

patterned relatively wide P-donor lines across the gap between two As^+-implanted fingers. Figure 2(a) shows a typical pattern where surface hydrogen has been completely desorbed by 7 V electrons from the STM tip within a 33 nm linewidth. Some of the bright protrusions on the rest of the surface are residual dangling bonds after H exposure (others are Si ad dimers). Most of these isolated sites are single dangling bonds that do not adsorb PH_3 molecules. As a result, resistance at a GΩ scale is maintained between the fingers after Si overgrowth with and without PH_3 exposure on *un*patterned templates.

Figure 2(b) shows 0.3 K *I-V* characteristics for 50 and 95 nm wide P-donor lines after PH_3 exposure and 2.8 nm Si overgrowth. The data for these samples shows a total ohmic resistance of 337 and 174 kΩ, respectively. Carriers in the nondegenerate *p*-type substrate are frozen out at this temperature, so electron conductance is totally confined to the P-donor line and the degenerately implanted fingers. To characterize the fingers, we fabricated a few test structures consisting of 1–4 continuous As^+-implanted lines of the same width as the fingers, connected to top and bottom pads. The resulting *I-V* characteristics yield an average resistance of $\sim$120 kΩ/line across 0.8 mm at 0.3 K, with a spread of $\sim$30 kΩ/line. From this average for the fingers, we infer a net P-donor line resistance of $\sim$220 and $\sim$50 kΩ for the 50 and 95 nm lines, respectively. These results do not appear to scale with inverse linewidth (even with the large uncertainty in finger resistance), and imply sheet resistances significantly greater than previously reported for unpatterned P δ layers.[2,3] These apparent discrepancies could be caused by a number of process variables that are not yet under accurate control, and/or unanticipated effects at the finger/line interfaces; or simply by increased boundary scattering in narrow lines. More measurements are in progress to clarify this situation. Nevertheless, the present process should be good enough to explore possibilities for high impedance devices like planar tunnel junctions and single-electron transistors. The maximum current passed through the 95 nm wire is 100 nA. Simulations of the P δ-layer indicate an electrical thickness of $\sim$4 nm,[9] so we find that this P-donor line can carry a current density of at least $\sim$25 kA/cm^2 at 4.2 K, comparable to the capacity of a highly doped Si nanowire.[10]

Magnetoresistance for the P-donor line samples was measured in a perpendicular magnetic field from 0 to 7 T at 0.3 K. Figure 3 compares the strong negative resistance peak at $B=0$ for an unpatterned P δ-layer with results for the 50 and 95 nm lines. This negative resistance peak is a weak localization effect due to diffusive scattering in a metallic 2DEG. From previous analysis, we infer an electron phase coherence length of $\sim$150 nm for the unpatterned P δ-layer. When the line width becomes less than the phase coherence length,

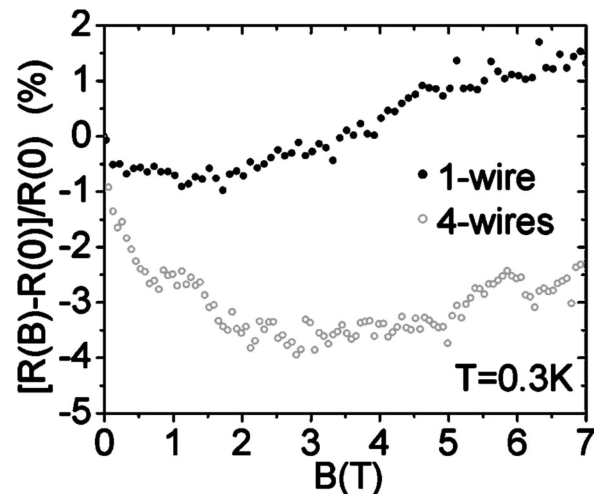

FIG. 5. Magnetoresistance change for the 1 and 4 Ga-acceptor wires at 0.3 K.

the 2D peak is expected to be suppressed and 1D localization theory should be applied. Both the 50 and 95 nm lines display significant deviations of this type from the magnetoresistance behavior of the δ layer. In addition, we find that the magnitude and functional form of the low-field magnetoresistance data for the two P lines are consistent with an earlier work by Choi *et al.*[11] where a wide channel (300 μm) and a narrow channel (0.2 μm) were etched into a high mobility GaAs/AlGaAs 2DEG system. This result implies that our Si nanofabrication process can provide an interesting way to investigate 1D weak localization in the diffusive regime where the phase coherence length is small. Similar results from a 90 nm P-donor line in Si have recently been reported by Rueß *et al.*[12] using a different approach where electrical contacts are applied after STM lithography.

IV. GA-ACCEPTOR WIRES

Direct ion implantation of nanometer scale features with a focused ion beam (FIB) presents a possible alternative to pattern definition by electron beam lithography.[13] In our case, FIB implants are attractive for connecting ~10 nm scale dopant patterns formed by STM lithography to micron size electrodes. Our ion-implanted template should provide a good initial test bed for exploring this approach. Figure 4(a) shows a 200 nm-wide wire implanted with 30 keV Ga^+ ions in a FEI Strata 235 dual beam FIB at a dose of $\sim 5 \times 10^{15}$ cm^{-2}, across a gap between As^+-implanted fingers. After annealing for 5 min at 600 °C in vacuum, the Ga-acceptor wires remain conducting at 0.3 K. *I-V* characteristics of samples containing 1 and 4 Ga wires of 0.2 μm width between As^+-implanted fingers are shown in Fig. 4(b). This system can be modeled as a double junction *n-p-n* structure with a degenerately doped Ga wire in the middle. With a nonzero bias, one junction is forward biased while the other is reverse biased, so the current is determined solely by the forward biased junction. The current for the four-wire sample is ~6 times higher than for the one-wire sample at a given bias, possibly due to small variations in the dose.

Figure 5 shows magnetoresistance at 0.3 K for Ga^+-implanted wires that is qualitatively different from the P-donor lines. Both Ga^+ samples exhibit negative magnetoresistance at low B field, but positive magneoresistance at high field. This behavior is similar to a previous report where a FIB line was patterned between BF^+ implanted contacts with 100 keV Ga^+ ions at a beam diameter of 0.1 μm.[14] To avoid nonlinear effects and accurately characterize FIB lines down to ~30 nm, we plan to repeat the same experiments with Ga^+-implanted contacts in the near future.

V. DISCUSSION AND CONCLUSIONS

We have demonstrated that Si templates with As^+-implanted contacts can be processed in UHV to generate atomically clean and flat surfaces for fabrication of epitaxial device structures. Here, low-energy electrons from a STM tip were used to pattern the H-terminated Si(100) surface and grow P-donor lines into the Si crystal lattice from PH_3 precursor molecules. Much of our future work will focus on possibilities for realizing planar tunnel junctions and single-electron transistors by inserting ~10 nm gaps into P-donor lines of this type. Electron transport and material properties of these structures will need to be understood more thoroughly before nanoscale devices can be reliably evaluated. The UHV process described here can be used to explore many of these issues. Samples containing FIB implants can be cleaned up to the same level as the templates shown in Fig. 1(c), opening additional opportunities to integrate focused-ion beams with STM-defined dopant patterns for prototyping small circuits.

Thus far, we have used STM for nanoscale lithography and for monitoring process development at the atomic level. Growing arrays of dopant atoms into the Si crystal lattice offers a natural extension of current technology to the atomic scale where quantum effects can be exploited. Other electron sources, such as low energy e-beam microcolumns, might be developed in the future for large-scale applications at sub-10 nm resolution if this approach turns out to be successful.

ACKNOWLEDGMENTS

The authors thank Dr. R. G. Clark for sharing unpublished results in Ref. 12. This work is supported by the DARPA-QuIST program under Contract No. DAAD19-01-1-0324, and ARO/ARDA under Contract No. DAAD19-01-1-0579.

[1]J. R. Tucker and T. C. Shen, Solid-State Electron. **42**, 1061 (1998).
[2]T.-C. Shen, J.-Y. Ji, M. A. Zudov, R.-R. Du, J. S. Kline, and J. R. Tucker, Appl. Phys. Lett. **80**, 1580 (2002). M. A. Zudov, C. L. Yang, R. R. Du, T.-C. Shen, J.-Y. Ji, J. S. Kline, and J. R. Tucker, cond-mat/0305482.
[3]L. Oberbeck, N. J. Curson, M. Y. Simmons, R. Brenner, A. R. Hamilton, S. R. Schofield, and R. G. Clark, Appl. Phys. Lett. **81**, 3197 (2002)
[4]S. R. Schofield, N. J. Curson, M. Y. Simmons, F. J. Rueß, T. Hallam, L. Overbeck, and R. G. Clark, Phys. Rev. Lett. **91**, 136104 (2003).
[5]J. C. Kim, J.-Y. Ji, J. S. Kline, J. R. Tucker, and T.-C. Shen, Appl. Surf. Sci. **220**, 293 (2003).
[6]W. Kern, Semicond. Int. **7**, 94 (1984).
[7]T.-C. Shen, J. S. Kline, and J. R. Tucker (unpublished).
[8]For a review of this technique, see T.-C. Shen and Ph. Avouris, Surf. Sci. **390**, 35 (1997).
[9]A. Fang, Y.-C. Chang, and J. R. Tucker (unpublished).
[10]N. Clement, A. Francinelli, D. Tonneau, Ph. Scotto, F. Jandard, H. Dallaporta, V. Safarov, D. Fraboulet, and J. Gautier, Appl. Phys. Lett. **82**, 1727 (2003).
[11]K. K. Choi, D. C. Tsui, and K. Alavi, Phys. Rev. B **36**, 7751 (1987).
[12]F. J. Rueß, L. Oberbeck, M. Y. Simmons, K. E. J. Goh, A. R. Hamilton, T. Hallam, N. J. Curson, and R. G. Clark (unpublished).
[13]J. Melngailis, J. Vac. Sci. Technol. B **5**, 469 (1987).
[14]H. Iwano, S. Zaima, T. Kimura, K. Matsuo, and Y. Yasuda, Jpn. J. Appl. Phys., Part 1 **33**, 7190 (1994).