Formation of 15 nm scale Coulomb blockade structures in silicon by electron beam lithography with a bilayer resist process

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We have formed Coulomb blockade structures with widths of 15–30 nm in silicon-on-insulator (SOI) by electron beam lithography (EBL) in a bilayer resist process. The bilayer structure consisted of HSQ (hydrogen silsesquioxane) and AZ organic resist. The organic resist protects the buried oxide and allows removal of exposed HSQ features with hydrofluoric acid (HF). Measurements at 4.2 K show pronounced Coulomb blockade signatures for 15 nm wide wires. This bilayer resist process provides direct lithographic access to 15 nm level features in SOI without the need for size reduction by oxidation. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1825012]

I. INTRODUCTION

Solid-state quantum devices are of interest as future electronic devices because of their low power consumption rate and huge potential for scalability.[1,2] Sensitive electrometers based on single electron transistors (SET) in silicon are attractive candidates for single spin readout through spin dependent charge measurements in proposed solid state quantum computation schemes.[3–6] Up to date, there have been many lithographic approaches to obtain ~10 nm scale devices including electron beam lithography, scanned probe lithography, and nanoimprints.[7–9] While integration of SETs into high density logic applications requires reliable room temperature operation, the usage of SETs in the context of quantum computing research allows operations at low temperatures. Charging energies of silicon SETs in the meV range allow process optimization at easily accessible liquid helium temperatures.[10,11] In this article we report on our development of an EBL process with a bilayer resist process that allows reliable formation of Coulomb blockade structures with 15 nm width in SOI.

II. FABRICATION OF NANOWIRES

In our approach for device fabrication, silicon-on-insulator (SOI) wafers with 400 nm buried oxide layers prepared by Smart Cut™ technology were used. The device region was thinned down to 30 nm by dry oxidation and then the top oxide layer was etched down to a thickness of 20 nm by timed dipping in HF solution. A silicon germanium layer of ~800 nm was deposited on the 20 nm oxide layer and patterned for formation of EBL markers for e-beam lithography. After patterning marker structures, the 20 nm oxide layer was removed by a timed HF dip. In order to obtain ultrathin nanowires, a hydrogen silsesquioxane (HSQ) and an organic (AZPN114) bilayer resist were used.[12] First, the organic resist was spun and baked (250 °C, 5 min, 90 nm thick). Then, on the organic resist layer, 1.8% HSQ resist was spun and soft baked (170 °C, 5 min, 30 nm). We defined nanowires of different sizes by EBL with a 100 keV electron beam (dose, 6000 $\mu C/cm^2$) in our Leica VB6HR. Nominal wire widths were 10 nm, 20 nm, and 30 nm with a length of 200 nm. HSQ resist was developed for 8 min in LDD-26w followed by O_2 plasma dry etching to define the second AZ organic resist layer. HSQ resist was used to transfer ultrathin patterns into organic resists. In order to protect the buried oxide of the SOI wafer from BHF dip (buffered HF solution) in the following process, 30 nm thick HSQ resist was stripped off by BHF dip before dry etching of the device region. After leaving the defined AZ organic resist, we etched the silicon device layer by plasma etching with hydrogen bromide chemistry. Here, the original structure of the organic resist on the buried oxide layer was maintained, while the patterns were transferred into the silicon device layer. The organic resist was then removed in a piranha bath (6000 ml surfuric acid bath heated to 120 °C added with 100 ml of hydrogen peroxide). We then implanted the nanowires and lead electrodes with phosphorous ions (10 keV) at a dose of 5×10^{14} cm^{-2}. This dose yields quasimetallic doping of source and drain electrodes and nanowires. Wafers were then annealed in a rapid thermal annealing chamber for dopant activation (nitrogen ambience, 1000 °C, 5 min). The exposed region, defined by EBL, was capped by a 30 nm thick CVD oxide and there were two electrode formation processes to fan out using highly doped polysilicon and aluminum layers.

III. RESULTS AND DISCUSSION

Figures 1(a)–1(c) show scanning electron microscope (SEM) images of nanowires after HSQ development in LDD-26w solution for 10 nm, 20 nm, and 30 nm, respectively. HSQ negative resist showed reproducible clean shapes down to 10 nm thin structures with small variations. In Fig. 2, the schematic diagram of the EBL process indicates all processes from resist deposition to wire formation. In Figs. 3(a) and 3(b), we show SEM pictures of wires with gate

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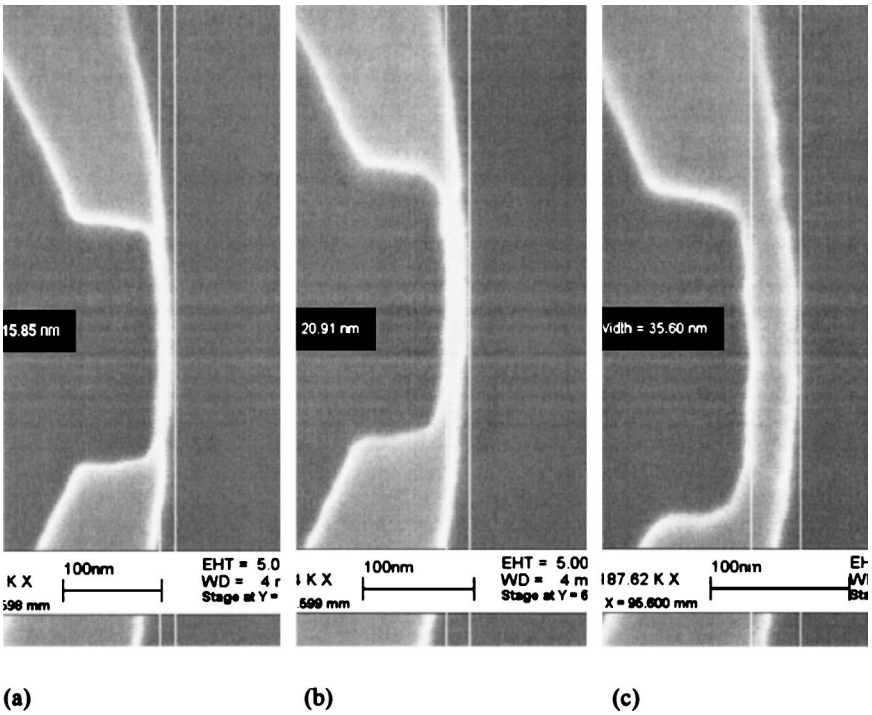

FIG. 1. Wire structures of (a) 16 nm, (b) 21 nm, and (c) 35 nm widths after developing HSQ. (Designed for 10 nm, 20 nm, and 30 nm of linewidth, respectively.)

electrodes located with a spacing of 100 nm from the wires. In these pictures, the actual 20 nm and 30 nm silicon wires are shown before removal of the patterned AZ organic resist. The actual width of the 20 nm wire pattern was thinned down to 15 nm. By comparing the SEM pictures in Fig. 3 with Fig. 1, it is evident that the organic resist is unstable for wires with widths below 20 nm in HSQ. AZ organic resist with a width of 20 nm can be defined by the oxygen plasma transfer process in serpentine shapes without any breakage during the HSQ removal process. However, resist patterns below 10 nm wire width were broken during HSQ removal and there were no wirelike patterns left. The thickness of the AZ organic resist was 90 nm, so that aspect ratios of 10, 20, and 30 nm wide wires were 1:9, 1:4.5, and 1:3, respectively. In Fig. 3, we show 15 nm and 30 nm wide wires transferred into silicon (step 5 in Fig. 2). The 15 nm wide wire shows a serpentine structure. We believe that this irregularity appears for wires with aspect ratios below 1:3 due to instability of the organic resist during oxygen plasma etching (step 2) or BHF dip (step 3). The 20 nm pattern in HSQ has lost some of its volume and the width of the wire pattern was reduced down to 15 nm as shown in Fig. 3(a). As a result of the following dry etching and dopant ion implantation processes, 15 nm and 30 nm patterns were fabricated into quasimetallic nanowire devices on the device layer. From Figs. 1 and 3, we could see small distortions in 15 nm wires and also ~25% volumetric loss in the organic resist. We suspect that the distorted shape of the organic resist following oxygen plasma etching and the BHF dip contributed to increased Coulomb blockade for the 15 nm wires.

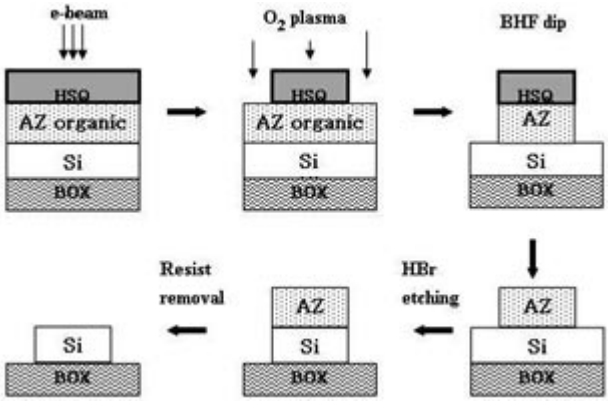

FIG. 2. Schematic diagram of resist formation processes through pattern transfer.

After forming all electrodes, Si-nanowires were tested in our cryostat. A HP-4156C parameter analyzer was used for these measurements. There was no signal from 10 nm wires in accordance with the results from SEM inspection. We have measured $I-V$ characteristics of the quantum wires at 4.2 K as shown in Fig. 4 with the goal of correlating the topographical structure with the electrical properties. Two silicon wires have the same lengths (200 nm) and heights (30 nm). The Coulomb blockade effect of the 30 nm wire was just barely visible for very small source drain voltages ($V_{s-d} \sim 3$ meV). For 15 nm wires, Coulomb blockade was much more pronounced with $\pm e/C \sim 20$ mV. Because the two wires were fabricated on the same wafer, the Coulomb blockade effects are expected to result from tunneling junctions formed in nanowires in two different widths. The 30 nm quantum wire shows a total junction capacitance of ~100 aF from the measured data with operational source and drain voltages less than 2 mV. At this condition, the one electron charging energy is 0.75 meV, which is only about

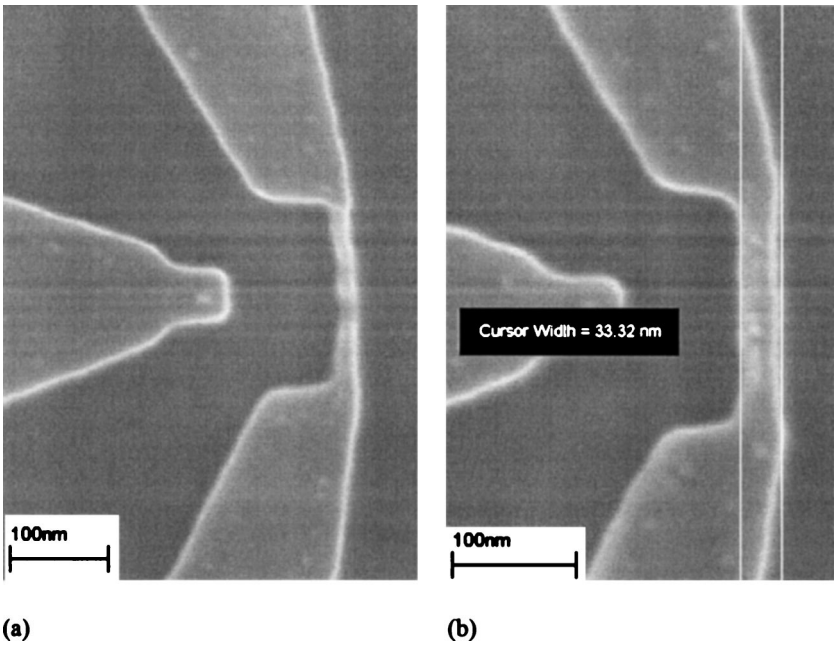

FIG. 3. Wires of (a) 15 nm and (b) 30 nm widths along with gate electrodes (100 nm spacing from nanowires) defined in the silicon device layer (after step 5 in Fig. 2).

double the thermal energy at 4.2 K, 0.36 meV (k_BT at 4.2 K, k_B; Boltzmann's constant). The 15 nm quantum wire showed a capacitance of ~15 aF and the charging energy, E_c, was 6 meV, assuming single electron charging of the nanowire, and Coulomb blockade is clearly visible because E_c is more than 15 times of the thermal energy at 4.2 K, the given temperature. The measurement data shown in Fig. 5 indicate source and drain current modulation with respect to the varying gate voltages (Vg) for a series of different source-drain biases, V_{s-d}. In Fig. 5(a), it was difficult to see discrete gate modulations from the 30 nm wire when measured with V_{s-d} of 5 mV, 10 mV, and 15 mV (from the bottom curve to the top one, respectively). The current oscillation by varying Vg is only ~1% of the total current with a period of at least ~1.2 V, which leads to gate capacitance of ~0.13 aF. However, in Fig. 5(b), devices with a 15 nm wire show a 75% gate modulation with a period of at least 200 mV of Vg. The capacitance of the gate (Cg) is estimated to be 8 aF. Coulomb blockade devices with 15 nm wire width are candidates for applications as sensitive electrometers.

IV. CONCLUSIONS

Electron beam lithography with a bilayer resist structure of HSQ and AZ organic resist allows formation of nanowire structures in SOI with widths down to 15 nm. This process allows direct lithographic access to Coulomb blockade structures without size reduction by thermal oxidation of nanowires. Dopant segregation during activation annealing and consecutive processes and variations of wire geometry from defects in the organic resist might contribute to tunnel junction formation. We speculate that multiple junctions can be formed in the middle of the 15 nm wire because of its rough sidewalls and dopant segregation effects. Several groups have reported strong dopant segregation effects for phosphorous in the vicinity of SiO_2/Si interfaces.[10,13] We suspect

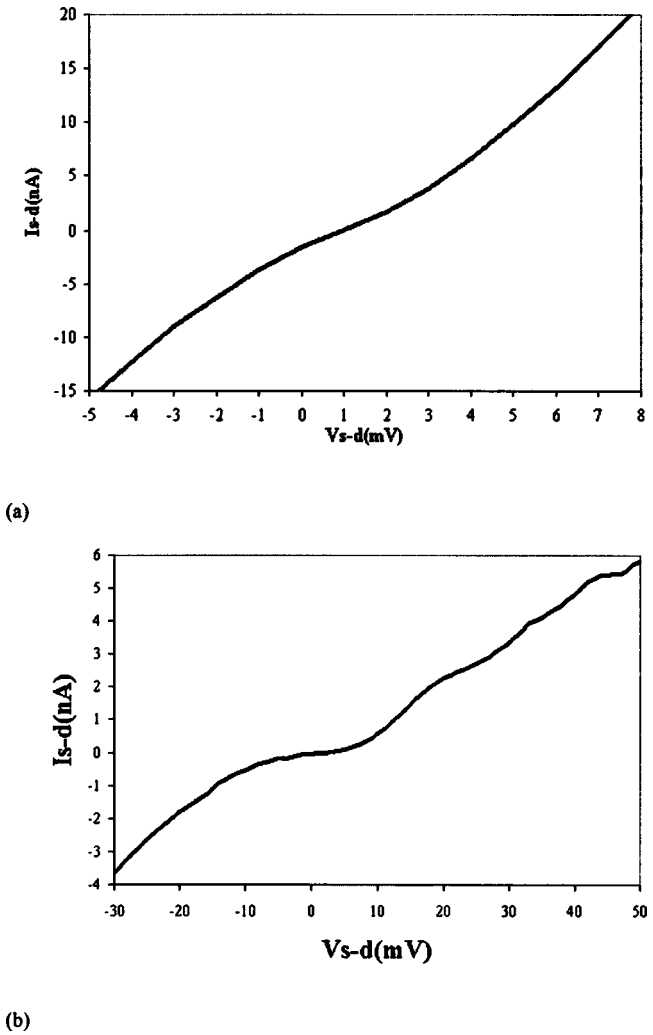

FIG. 4. Source and drain current (I_{s-d}) as a function of source–drain voltage measurement data with varying V_{s-d} for devices with (a) 30 nm and (b) 15 nm wide wires.

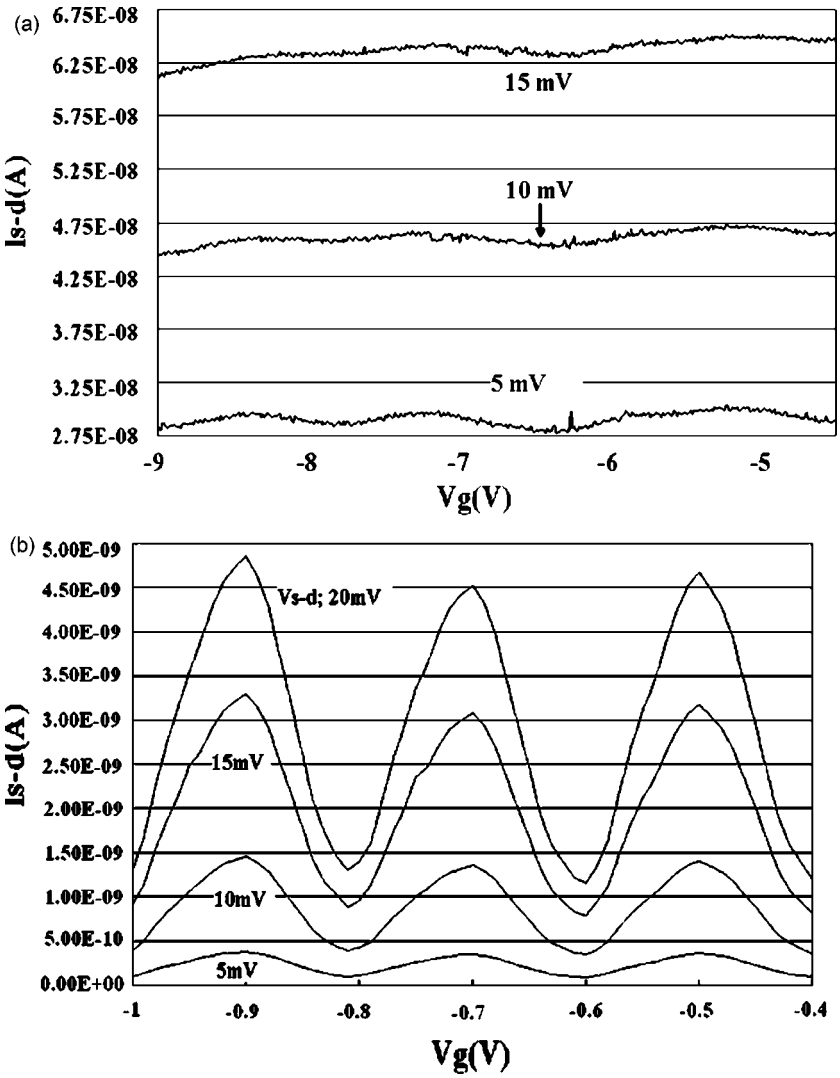

FIG. 5. Source and drain current (I_{s-d}) as a function of measurement data with varying gate bias V_g for devices with (a) 30 nm and (b) 15 nm wires at different V_{s-d} as indicated.

that the rough sidewall of the 15 nm wires increased the actual area facing the surrounding oxide layers of the burried oxide and cap oxide. Dopant segregation can transform the uniform dopant concentration along the wire and result in isolated regions and this might contribute to the formation of multiple tunnel junctions in narrow nanowires. Ongoing studies aim at correlating electrical properties of nanowire devices with process parameters, nanowire geometries, and the application of SETs as sensitive electrometers for quantum bit readout.[3–6]

ACKNOWLEDGMENTS

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